S2IMAC External Peripheral Controller (EPC) v1.02a

DS031 February 25, 2011

Product Extension Specification

Introduction

This specification defeines the extension to the original XPS EPC IP Core by Xilinx. The original controller supports data transfers between the Processor Local Bus (PLB V4.6) and the external synchronous and / or asynchronous peripheral devices such as USB and LAN devices.

As well as the original controller the S2IMAC EPC supports peripheral devices in the same manner and closes the leak of dowdy interrupt handling.

CORE Facts		
Core Specifics		
Supported Device Family	Virtex®-6, Spartan®-6, Virtex-5/5FX, Virtex-4/4QV/4Q, Automotive Spartan-3/3A/3A DSP/3E, Spartan-3E, Spartan-3, Spartan-3A, Spartan-3A DSP	
Version of Core	s2imac_epc	v1.02a
Resources Used		
	Min	Max
Slices	Refer to DS581 to Table 5, Table 6. Table 7 and TaDS581ble 8	
LUTs		
FFs		
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Design Tool Requirement		
Xilinx Implementation Tools	ISE® 11.3 or later	
Verification	–	
Simulation	–	
Synthesis	XST	
Support		
Provided by Xilinx, Inc. for the XPS EPC part. Provided by Li-Pro.Net for the S2IMAC EPC part.		

Features

S2IMAC Extension

- Single Interrupt Handling (simple pass-through)

XPS EPC Standard Features

- Connects as a 32-bit slave on PLB V4.6 buses of 32-bit, 64-bit or 128-bit
- PLB interface with byte enable support
- Parameterized support of up to four external peripheral devices with each device configured with separate base address and high address range
- Supports both synchronous and asynchronous access modes of peripheral devices with the support for a separate clock domain for synchronous peripheral devices
- Supports both multiplexed and non-multiplexed address and data buses
- The data width of peripheral devices is independently configured to 8-bit, 16-bit or 32-bit with the provision to enable data width matching when the PLB data width is greater than that of peripheral device
- Configurable timing parameters for peripheral bus interface

Functional Description

The S2IMAC External Peripheral Controller (S2IMAC EPC) is based on Xilinx's original IP Core XPS EPC. The interface diagram shown in Figure 1 depicts the overall interfaces of the core design. New in S2IMAC is the fast forward pass-through of a single interrupt line on top level.

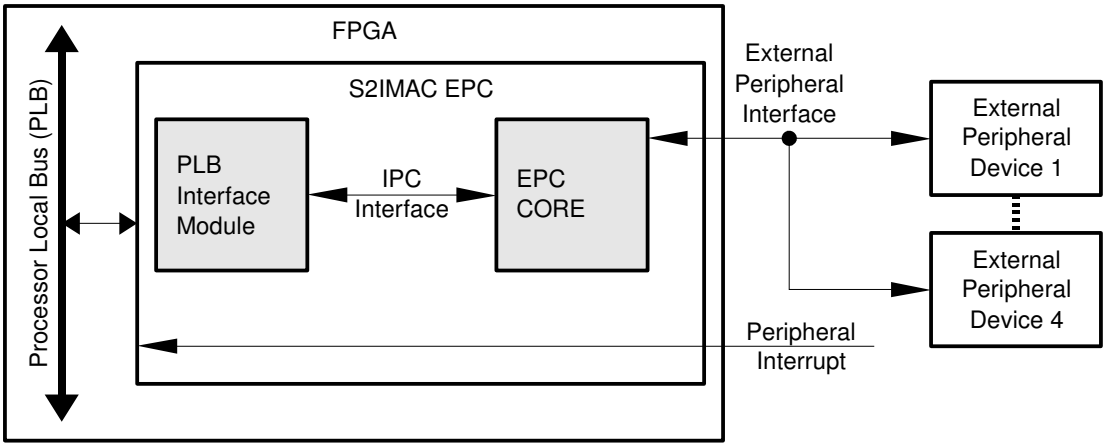

Figure 1: **S2IMAC EPC Interface Diagram**

As well as the XPS EPC the S2IMAC EPC IP Core design provides a general purpose interface to external peripheral devices and the PLB. The S2IMAC EPC IP Core can be configured to provide support for multiple external peripherals (non-memory peripherals like USB, LAN etc.) up to maximum of four devices. For more functional description read Xilinx original product specification DS581.

As a new extension the S2IMAC EPC provides a simple pass-through handling for a single peripheral interrupt line. There is no interrupt control functionality.

S2IMAC EPC IP Core Design Parameters

To allow user to create the S2IMAC EPC that is uniquely tailored for the user´s system, certain feature can be parameterized in the S2IMAC EPC design. All the design parameters presented by XPS EPC are represented by S2IMAC EPC. For more informations read Xilinx original product specification DS581.

The additional feautures that are parameterizable in the extended S2IMAC EPC core are as shown in Table 1.

Table 1: **S2IMAC EPC IP Core Extended Design Parameters**

Generic	Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
S2IMAC EPC Extended Interface Paraemters					
G41	S2IMAC Interrupt	C_INTERRUPT_ PRESENT	0 = Interrupt pass-through ist not present 1 = Interrupt pass-through is present	0	integer

S2IMAC EPC IP Core I/O Signals

The extended S2IMAC EPC core I/O signals are listed and described in the Table 2.

Table 2: **S2IMAC EPC IP Core Extended Design Parameters**

Port	Signal Name	Interface	Signal Type	Initial State	Description
S2IMAC EPC Extended Signals					
P57	PRH_Int	S2IMAC	I	–	External peripheral interrupt input
P58	IP2INTC_Irpt	S2IMAC Interrupt	O	0	S2IMAC Interrupt Active high signal

Parameter – Port Dependencies

In addition, when certian features are parameterized away, the related logic is removed. The dependencies between the S2IMAC EPC extended design parameters and the I/O ports are shown in Table 3.

Table 3: **S2IMAC EPC IP Core Extended Parameter – Port Dependencies**

Generic or Port	Parameter	Affects	Depends	Relationship Description
G41	C_INTERRUPT_PRESENT	P57, P58	–	When C_INTERRUPT_PRESENT is 1, interrupt input is connected to interrupt output. Otherwise the interrupt output is driven with an inactive level and the input is unused.

Specification Exceptions

N/A

Support

Xilinx provides technical support for XPS EPC IP Core when used as described in the product documentation. For more informations read Xilinx original product specification DS581. Li-Pro.Net provides limited support for the S2IMAC EPC IP Core when used in commercial relationship between Li-Pro.Net and its customers.

Reference Documents

The following documents contain information that may be required in understanding the S2IMAC EPC IP Core reference designs:

1. DS581 XPS External Peripheral Controller (EPC), Product Specification version 2.0
2. IBM CoreConnect 128-Bit Processor Local Bus: Architecture Specifications version 4.6

Revision History

Date	Version	Revision
2/25/11	1.0	Initial Li-Pro.Net release.

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