XPS SYSACE (System ACE) Interface Controller (v1.01a)

DS583 July 20, 2009 **Product Specification**

Introduction

The XPS System ACE Interface Controller (or, interchangeably, the XPS SYSACE) is the interface between the Processor Local Bus (PLB) and the Microprocessor Interface (MPU) of the System ACE™ Compact Flash solution peripheral. This module attaches to the PLB.

Features

- Connects as a 32-bit slave on PLB V4.6 buses, which are 32, 64 or 128 bit wide
- The XPS SYSACE is used in conjunction with a System ACE Compact Flash Solution to provide a System ACE memory solution
- System ACE Microprocessor Interface (MPU)
  - Read/Write from or to a Compact Flash device
  - Supports both 8-bit and 16-bit data bus access modes

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	See EDK Supported Device Families.	
Version of Core	xps_sysace	v1.01a
Resources Used		
	Min	Max
Slices	Refer to the Table 7, Table 8, Table 9, Table 10 and Table 11	
LUTs		
FFs		
Block RAMs	N/A	
Special Features	N/A	
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	N/A	
Verification	N/A	
Instantiation Template	N/A	
Additional Items	N/A	
Design Tool Requirements		
Xilinx Implementation Tools	See Tools for requirements.	
Verification		
Simulation		
Synthesis		
Support		
Provided by Xilinx, Inc.		

Functional Description

The XPS SYSACE is composed of the PLB Interface module and the System ACE Interface Controller. The connections between the XPS System ACE Interface Controller, the PLB Interface module, and the Xilinx System ACE Controller device are shown in Figure 1

The XPS SYSACE provides the MPU interface to the Xilinx System ACE Controller Device. The Xilinx System ACE Controller device has multiple interfaces, including CompactFlash, MPU and JTAG. This allow for a highly flexible configuration solution. The MPU interface of the Xilinx System ACE Controller device is composed of a set of registers that provide a means for communicating with CompactFlash control logic, configuration control logic, and other resources in the Xilinx System ACE Controller device. Specifically, this interface can be used to read the identity of a CompactFlash device and read/write sectors. The XPS System ACE Interface Controller provides a means of communicating with the registers and data buffers that correspond to the CompactFlash device in the Xilinx System ACE Controller device, via the PLB. Refer to the System ACE Interface Controller Flash chip document mentioned in the Reference Documents section for detailed information on the operation of the MPU interface, the MPU interface register definitions, and the MPU interface register address map.

The XPS System ACE Interface Controller allows for the registers and data buffers of the Xilinx System ACE Controller device, to be accessed in a 8-bit and 16-bit data bus access mode. The two modes are differentiated by the means of the parameter C_MEM_WIDTH, as follows:

- 8-bit mode(C_MEM _WIDTH = 8): The registers are accessed in a 8-bit data bus access mode. In this mode, the registers of the Xilinx System ACE Controller device should be accessed via byte accesses only.
- 16-bit mode(C_MEM _WIDTH = 16): The registers are accessed in a 16-bit data bus access mode. In this mode, the registers of the Xilinx System ACE Controller device should be accessed via halfword accesses only.

For example, a typical register like the Bus Mode register, is accessed by addresses "00h" and "01h" in the 8-bit access mode. It would be accessed by address "00h" in the 16-bit access mode.

The software drivers use the C_MEM_WIDTH parameter to configure the Xilinx System ACE Bus Mode register (setting the Xilinx System ACE MPU data bus access width to the desired mode) and to access the registers with the proper type of transaction.

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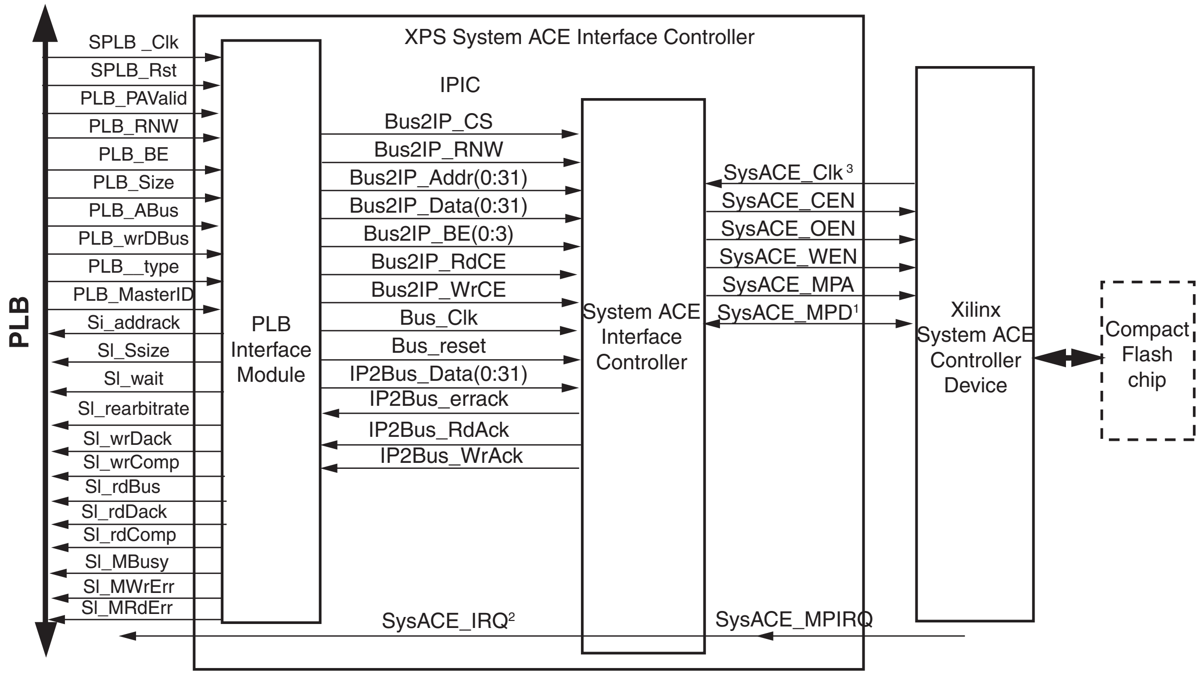

Notes:

1. SysACE_MPD is formed in the IOB from SysACE_MPD_I, SysACE_MPD_0, and SysACE_MPD_T.
2. SysACE_IRQ should be connected to the interrupt input of the processor.
3. SysACE_Clk should be connected to a global clock buffer by the user.

Figure 1: **XPS System ACE Interface Controller Block Diagram**

PLB Interface Module

PLB Interface Module provides an interface between XPS System ACE Interface Controller and the PLB. The PLB Interface Module implements the basic functionality of a PLB slave and does the necessary protocol and timing translation between the PLB and the IPIC interface. PLB Interface Module supports only single beat transactions.

System ACE Interface Controller

The System ACE interface controller contains a controller state machine and logic to synchronize signals across the SPLB_Clk and SysACE_Clk domains as shown in Figure 2.

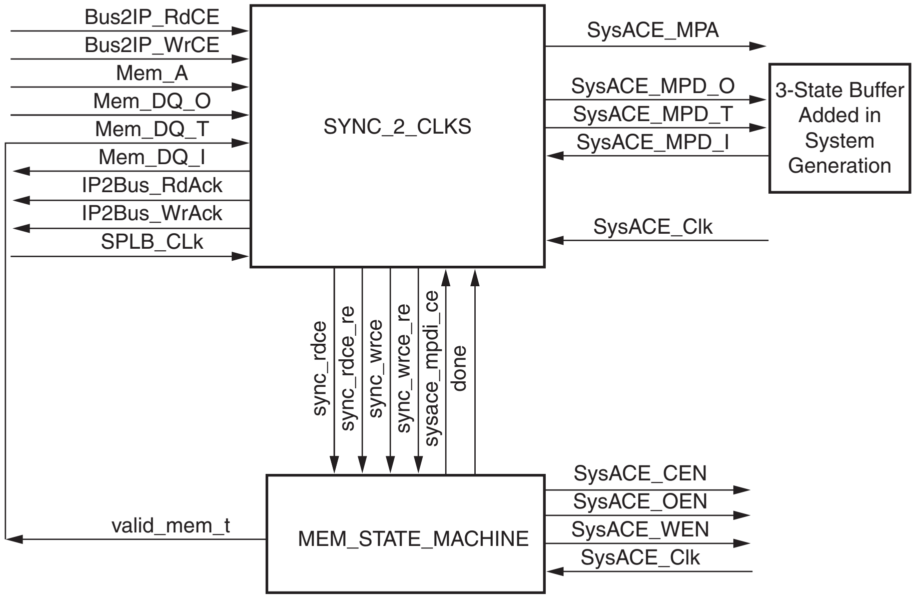

Figure 2: **System ACE Interface Controller Diagram**

The XPS System ACE Interface Controller core does not contain any internal registers or addressable memory space, therefore the mapping of PLB address bus is one-to-one with the System ACE address bus (SysACE_MPA) as shown in Table 1.

Table 1: **PLB Address Bus to System ACE Address Bus Mapping (done in IP core)**

PLB Address Bus	System ACE Address Bus
PLB_ABus[25 : 31]	SysACE_MPA[6 : 0]

The Xilinx System ACE Compact Flash chip is a true little-endian device and the PLB is a big-endian bus. Therefore the XPS System ACE Interface Controller will do a bit-swap in each byte when connecting the PLB data bus to the System ACE data bus as shown in Table 2.

Table 2: **PLB Data Bus to System ACE Data Bus Mapping (done in IP core)**

PLB Data Bus	System ACE Data Bus
PLB_DBus[8 : 15]	SysACE_MPD[15 : 8]
PLB_DBus[0 : 7]	SysACE_MPD[7 : 0]

Note however, that the XPS System ACE Interface Controller does not perform the byte swapping necessary to interface to a little-endian device when configured to use 16-bit mode. Therefore, the software drivers provided for this core will perform the necessary byte-swapping to correctly interface to the Xilinx System ACE Compact Flash chip as shown in Table 3.

Table 3: **PLB Big Endian to System ACE Little Endian Conversion (done in software driver)**

Byte	PLB Data Bus	System ACE Data Bus
MSB	PLB_DBus[0 : 7]	SysACE_MPD[15 : 8]
LSB	PLB_DBus[8 : 15]	SysACE_MPD[7 : 0]

Clocking - SYNC_2_CLKS Module

The controller state machine runs on the SysACE_Clk. The IPIC signals indicating the start of a transaction are synchronized to the System ACE clock and used to start the state machine. All address, data and control signals that are output to the System ACE Compact Flash chip are synchronized to the SysACE_Clk and registered in the FPGA IO registers using SysACE_Clk to ensure a clean interface between this chip and the FPGA. Data from the System ACE Compact Flash chip is also registered in FPGA IO registers using SysACE_Clk. It is then synchronized to the SPLB_Clk for transmission on the bus. The frequency of the SysACE_Clk must be less than the frequency of the SPLB_Clk.

Note that the address and data (if a write transaction) from the PLB will stay stable during the entire bus transaction and therefore would not have to be synchronized and output using the SysACE_Clk. This was done to provide a robust design, however, if the overall FPGA design is limited on resources, these synchronization registers could possibly be removed. The user is cautioned to analyze timing before removing these registers.

Also note that this core does not instantiate a global clock buffer for SysACE_Clk. This is left for the user to instantiate based on the resource requirements of their system.

System ACE Control state machine - MEM_STATE_MACHINE Module

The state machine in the System ACE Interface controller performs the specified transaction to the MPU interface of System ACE Compact Flash chip and is shown in Figure 3. This state machine is clocked by SysACE_Clk and therefore outputs all System ACE control signals synchronous to this clock. The input control signals from the PLB Interface Module have been synchronized to the SysACE_Clk in the sync_2_clocks module.

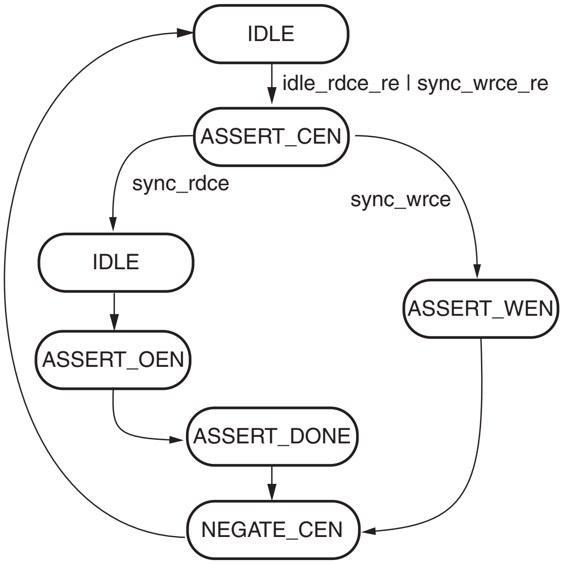

Figure 3: **System ACE Interface Control State Machine**

XPS System ACE Interface Controller I/O Signals

The I/O signals for the XPS System ACE Interface Controller are listed and described in Table 4.

Table 4: **XPS System ACE Interface Controller I/O Signals**

Port	Signal Name	Interface	I/O	Initial State	Description
System Signals					
P1	SPLB_Clk	PLB	I	-	PLB clock
P2	SPLB_Rst	PLB	I	-	PLB reset, active high
PLB Interface Signals					
P3	PLB_ABus[0 : C_SPLB_AWIDTH - 1]	PLB	I	-	PLB address bus
P4	PLB_PAValid	PLB	I	-	PLB primary address valid
P5	PLB_MasterID[0 : C_SPLB_MID_WIDTH - 1]	PLB	I	-	PLB current master identifier
P6	PLB_RNW	PLB	I	-	PLB read not write
P7	PLB_BE[0 : C_SPLB_DWIDTH/8 - 1]	PLB	I	-	PLB byte enables
P8	PLB_Size[0 : 3]	PLB	I	-	PLB size of requested transfer
P9	PLB_type[0 : 2]	PLB	I	-	PLB transfer type
P10	PLB_wrDBus[0 : C_SPLB_DWIDTH - 1]	PLB	I	-	PLB write data bus
Unused PLB Interface Signals					
P11	PLB_UABus[0 : C_SPLB_AWIDTH - 1]	PLB	I	-	PLB Upper Address bits
P12	PLB_SAValid	PLB	I	-	PLB secondary address valid
P13	PLB_rdPrim	PLB	I	-	PLB secondary to primary read request indicator
P14	PLB_wrPrim	PLB	I	-	PLB secondary to primary write request indicator
P15	PLB_abort	PLB	I	-	PLB abort bus request
P16	PLB_busLock	PLB	I	-	PLB bus lock
P17	PLB_MSize[0 : 1]	PLB	I	-	PLB data bus width indicator
P18	PLB_TAttribute[0 : 15]	PLB	I	-	PLB transfer attribute
P19	PLB_lockerr	PLB	I	-	PLB lock error
P20	PLB_wrBurst	PLB	I	-	PLB burst write transfer
P21	PLB_rdBurst	PLB	I	-	PLB burst read transfer

Table 4: **XPS System ACE Interface Controller I/O Signals *(Contd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P22	PLB_wrPendReq	PLB	I	-	PLB pending bus write request
P23	PLB_rdPendReq	PLB	I	-	PLB pending bus read request
P24	PLB_rdPendPri[0 : 1]	PLB	I	-	PLB pending write request priority
P25	PLB_wrPendPri[0 : 1]	PLB	I	-	PLB pending read request priority
P26	PLB_reqPri[0 : 1]	PLB	I	-	PLB current request priority
PLB Slave Interface Signals					
P27	Sl_addrack	PLB	O	0	Slave address acknowledge
P28	Sl_Ssize[0 : 1]	PLB	O	0	Slave data bus size
P29	Sl_wait	PLB	O	0	Slave wait
P30	Sl_rearbitrate	PLB	O	0	Slave bus rearbitrate
P31	Sl_wrDack	PLB	O	0	Slave write data acknowledge
P32	Sl_wrComp	PLB	O	0	Slave write transfer complete
P33	Sl_rdBus[0 : C_SPLB_DWIDTH - 1]	PLB	O	0	Slave read data bus
P34	Sl_rdDack	PLB	O	0	Slave read data acknowledge
P35	Sl_rdComp	PLB	O	0	Slave read transfer complete
P36	Sl_Mbusy[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave busy
P37	Sl_MWrErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave write error
P38	Sl_MRdErr[0 : C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Slave read error
Unused PLB Slave Interface Signals					
P39	Sl_wrBTerm	PLB	O	0	Slave terminate write burst transfer
P40	Sl_rdWdAddr[0 : 3]	PLB	O	0	Slave read word address
P41	Sl_rdBTerm	PLB	O	0	Slave terminate read burst transfer
P42	Sl_MIRQ[0:C_SPLB_NUM_MASTERS - 1]	PLB	O	0	Master interrupt request
System ACE Signals					

Table 4: **XPS System ACE Interface Controller I/O Signals** ***(Contd)***

Port	Signal Name	Interface	I/O	Initial State	Description
P43	SysACE_Clk[1]	System Ace Core	I	-	System ACE Clock
P44	SysACE_MPIRQ	System Ace Core	I	-	System ACE Active high Interrupt Input
P45	SysACE_CEN	System Ace Core	O	1	System ACE Chip Enable
P46	SysACE_OEN	System Ace Core	O	1	System ACE Enable
P47	SysACE_WEN	System Ace Core	O	1	System ACE Write Enable
P48	SysACE_MPA[6 : 0]	System Ace Core	O	0	System ACE Address
P49	SysACE_MPD_I[C_MEM_WIDTH-1 : 0]	System Ace Core	I	-	System ACE Data Input
P50	SysACE_MPD_O[C_MEM_WIDTH-1 : 0]	System Ace Core	O	0	System ACE Data Ouput
P51	SysACE_MPD_T[C_MEM_WIDTH-1 : 0]	System Ace Core	O	1	System ACE Data Output enable
P52	SysACE_IRQ[2]	System Ace Core	O	0	System ACE Active High Interrupt Output

Notes:

1. SPLB_Clk frequency must be greater than or equal to SysACE_Clk Frequency
2. This interrupt output is just a pass-through of the System ACE interrupt (SysACE_MPIRQ) and should be connected to an interrupt controller or directly to the processor's interrupt input

XPS System ACE Interface Controller Design Parameters

To allow the designer to obtain a XPS SYSACE core that is uniquely tailored for the designer's system, certain features can be parameterized. Some of these parameters control the interface to the PLB interface module while others provide information to minimize resource utilization. The features that can be parameterized in the XPS SYSACE are shown in Table 5.

Table 5: **XPS System ACE Interface Controller Parameters**

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameter					
G1	Target FPGA family	C_FAMILY	See C_FAMILY parameter values.		string
PLB Parameters					
G2	PLB System ACE Base Address	C_BASEADDR	Valid Address[1]	None [1]	std_logic_vector
G3	PLB System ACE High Address	C_HIGHADDR	Valid Address[1]	None[1]	std_logic_vector

Table 5: **XPS System ACE Interface Controller Parameters *(Contd)***

Generic	Feature/Description	Parameter Name	Allowable Values	Default Value	VHDL Type
G4	PLB address width	C_SPLB_AWIDTH	32	32	integer
G5	PLB data width	C_SPLB_DWIDTH	32, 64, 128	32	integer
G6	Selects point-to-point or shared bus topology	C_SPLB_P2P	0 = Shared Bus Topology	0	integer
G7	PLB Master ID Bus Width	C_SPLB_MID _WIDTH	$\log_2$(C_SPLB_ NUM_MASTERS) with a minimum value of 1	8	integer
G8	Number of PLB Masters	C_SPLB_NUM _MASTERS	1 - 16	3	integer
G9	Width of the Slave Data Bus	C_SPLB_NATIVE _DWIDTH	32	32	integer
G10	Selects the transactions as being single beat or burst	C_SPLB_SUPPORT _BURSTS	0 = Supports only single beat transactions	0	integer
System ACE Parameters					
G11	System ACE MPU Data Bus Access Mode[2]	C_MEM_WIDTH	8, 16	16	integer

Notes:

1. The range specified by C_BASEADDR and C_HIGHADDR must be sized and aligned to some power of 2, 2^n . Then, the n least significant bits of C_BASEADDR is zero. This range needs to encompass the addresses needed by the XPS SYSACE registers
2. Please refer to Xilinx DS080, System ACE Compact Flash Solution, for more information

Allowable Parameter Combinations

The address-range size of the XPS System ACE Interface Controller must be a power of 2. If the desired address-range size is represented by 2^n, then the n least significant bits of the base address must be 0. C_BASEADDR and C_HIGHADDR must specify an address range whose size is atleast 0x80, to cover the addressable registers and data buffer available in the Xilinx System Ace Compact Flash chip.

XPS System ACE Interface Controller Parameter-Port Dependencies

The dependencies between the XPS System ACE Interface Controller design parameters and I/O signals are described in Table 6. In addition, when certain features are parameterized out of the design, the related logic will no longer be a part of the design. The unused input signals and related output signals are set to a specified value.

Table 6: **XPS System ACE Interface Controller Parameter-Port Dependencies**

Generic or Port	Parameter	Affects	Depends	Relationship Description
Design Parameters				
G4	C_SPLB_AWIDTH	P3	-	Width of the PLB Address Bus
G5	C_SPLB_DWIDTH	P7, P10, P33	-	Width of the PLB Data Bus

Table 6: **XPS System ACE Interface Controller Parameter-Port Dependencies *(Contd)***

Generic or Port	Parameter	Affects	Depends	Relationship Description
G7	C_SPLB_MID_DWIDTH	P5	G8	Width of Master ID Bus
G8	C_SPLB_NUM_MASTERS	P36,P37, P38	-	The number of Master Devices connected to PLB bus
G11	C_MEM_WIDTH	P49, P50, P51	-	Width of the System ACE Data Bus
I/O Signals				
P3	PLB_ABus	-	G4	Width varies with the width of the PLB Address Bus
P5	PLB_MasterID	-	G7	Width varies with the MID width
P7	PLB_BE	-	G5	Width varies with the width of the PLB Data Bus
P10	PLB_wrDBus	-	G5	Width varies with the width of the PLB Data Bus
P33	Sl_rdBus	-	G5	Width varies with the width of the PLB Data Bus
P36	Sl_MBusy	-	G8	Width varies with the number of masters
P37	Sl_MWrErr	-	G8	Width varies with the number of masters
P38	Sl_MRdErr	-	G8	Width varies with the number of masters
P49	SysACE_MPD_I	-	G11	Width varies with the width of the System ACE Data Bus
P50	SysACE_MPD_O	-	G11	Width varies with the width of the System ACE Data Bus
P51	SysACE_MPD_T	-	G11	Width varies with the width of the System ACE Data Bus

XPS System ACE Timing Diagrams

This section contains timing diagrams showing the register read and write accesses to the Xilinx System ACE Interface controller. Note that the System ACE clock is not driven from this core, it is an input to this core. Also note the byte swapping that occurs during the register accesses. The Figure 4 and Figure 5 show the 8-bit register write and read cycles.

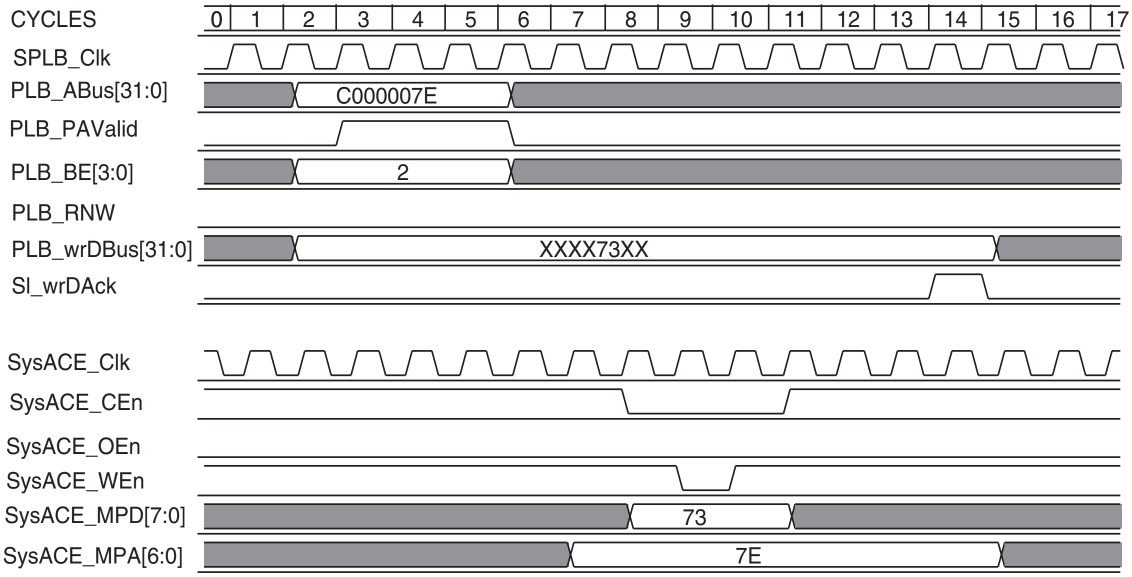

Figure 4: **XPS System ACE 8-bit Register Write**

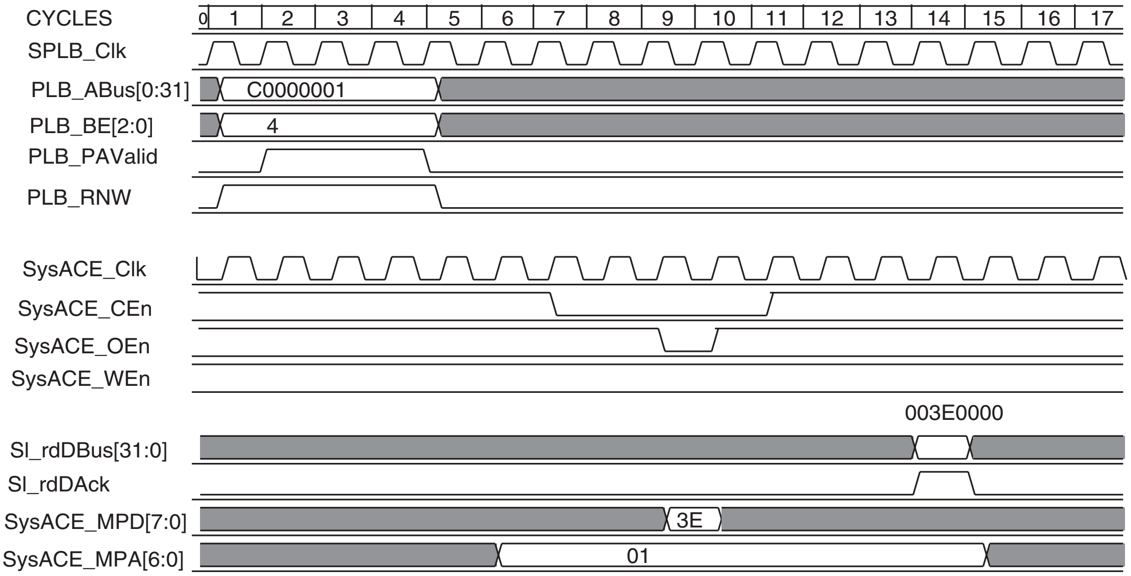

Figure 5: **XPS System ACE 8-bit Register Read**

Figure 6 and Figure 7 show the 16-bit register write and read cycles.

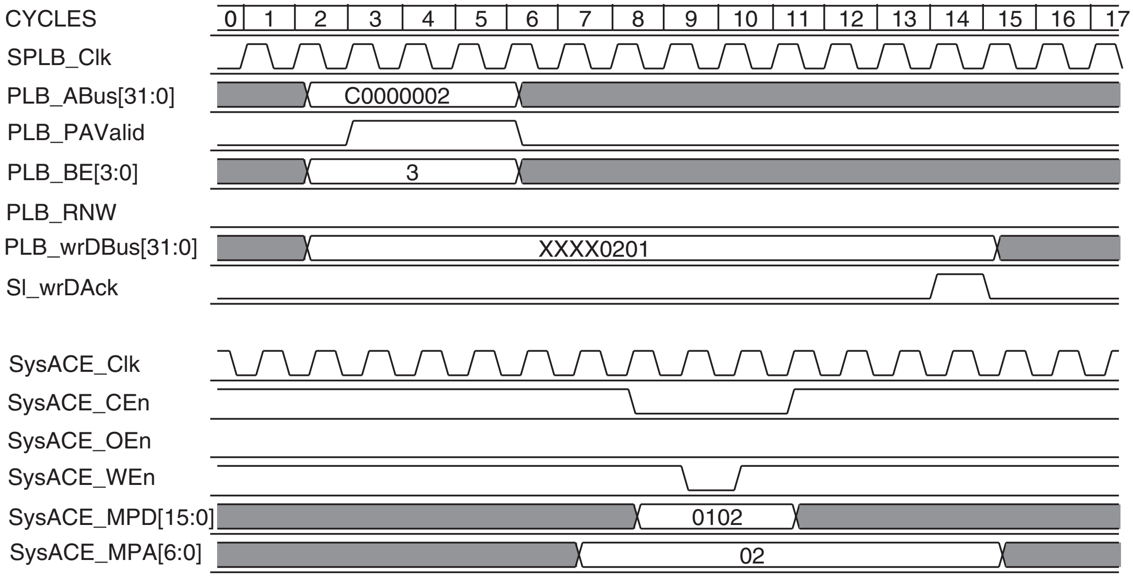

Figure 6: **XPS System ACE 16-bit Register Write**

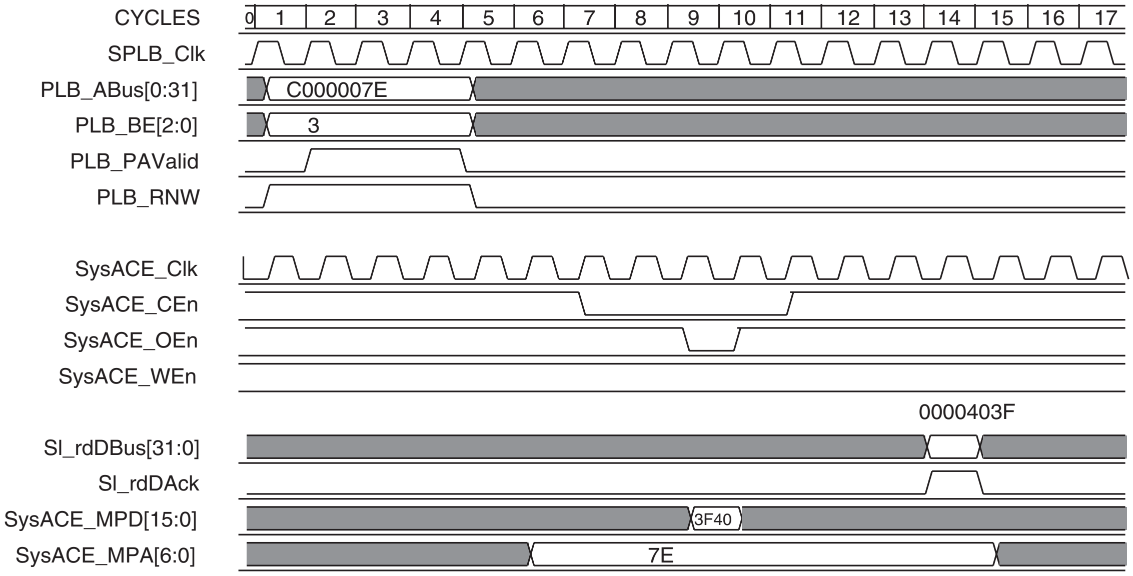

Figure 7: **XPS System ACE 16-bit Register Read**

Design Implementation

Target Technology

The target technology is an FPGA listed in EDK Supported Device Families.

Device Utilization and Performance Benchmarks

Core Performance

Since the XPS System ACE Controller will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are just estimates. When the XPS System ACE Interface Controller is combined with other designs in the system, the utilization of FPGA resources and timing will vary from the results reported here.

The XPS System ACE Interface Controller benchmarks are shown in Table 7, Table 8, Table 9, Table 10 and Table 11 for Virtex®-4, Virtex-5, Spartan®-3adsp, Virtex-6 and Spartan-6 FPGAs respectively.

Table 7: **Performance and Resource Utilization Benchmarks for Virtex-4 (xc4vlx40-ff668-10)**

Parameter Values			Device Resources			Performance
C_MEM_WIDTH	C_BASEADDR	C_HIGHADDR	Slices	Slice Flip-Flops	LUTs	F_{max} (in MHz)
8	30000000	3FFFFFFF	204	287	147	145.815
16	30000000	3FFFFFFF	218	313	148	145.603

Table 8: **Performance and Resource Utilization Benchmarks for Virtex-5 (xc5vlx30-ff676-1)**

Parameter Values			Device Resources		Performance
C_MEM_WIDTH	C_BASEADDR	C_HIGHADDR	Slice Flip-Flops	LUTs	F_{max} (in MHz)
8	30000000	3FFFFFFF	287	112	213.129
16	30000000	3FFFFFFF	311	111	212.089

Table 9: **Performance and Resource Utilization Benchmarks for Spartan-3adsp (xc3sd3400a-fg676-4)**

Parameter Values			Device Resources			Performance
C_MEM_WIDTH	C_BASEADDR	C_HIGHADDR	Slices	Slice Flip-Flops	LUTs	F_{max} (in MHz)
8	30000000	3FFFFFFF	240	287	117	124.301
16	30000000	3FFFFFFF	252	311	109	102.828

Table 10: **Performance and Resource Utilization Benchmarks for Virtex-6 (xc6vlx130t-1-ff1156)**

Parameter Values			Device Resources			Performance
C_MEM_WIDTH	C_BASEADDR	C_HIGHADDR	Slices	Slice Flip-Flops	LUTs	F_{max} (in MHz)
8	30000000	3FFFFFFF	78	268	188	257
16	30000000	3FFFFFFF	75	343	233	267

Table 11: **Performance and Resource Utilization Benchmarks for Spartan-6 (xc6slx45t-2-fgg484)**

Parameter Values			Device Resources			Performance
C_MEM_WIDTH	C_BASEADDR	C_HIGHADDR	Slices	Slice Flip-Flops	LUTs	F_{max} (in MHz)
8	30000000	3FFFFFFF	74	268	168	153
16	30000000	3FFFFFFF	83	344	216	151

System Performance

To measure the system performance (F_{MAX}) of this core, this core was added to a Virtex-4 system, a Virtex-5 system, and a Spartan-3ADSP system as the Device Under Test (DUT) as shown in Figure 8, Figure 9, and Figure 10.

Because the XPS SYSACE Controller core will be used with other design modules in the FPGA, the utilization and timing numbers reported in this section are estimates only. When this core is combined with other designs in the system, the utilization of FPGA resources and timing of the core design will vary from the results reported here.

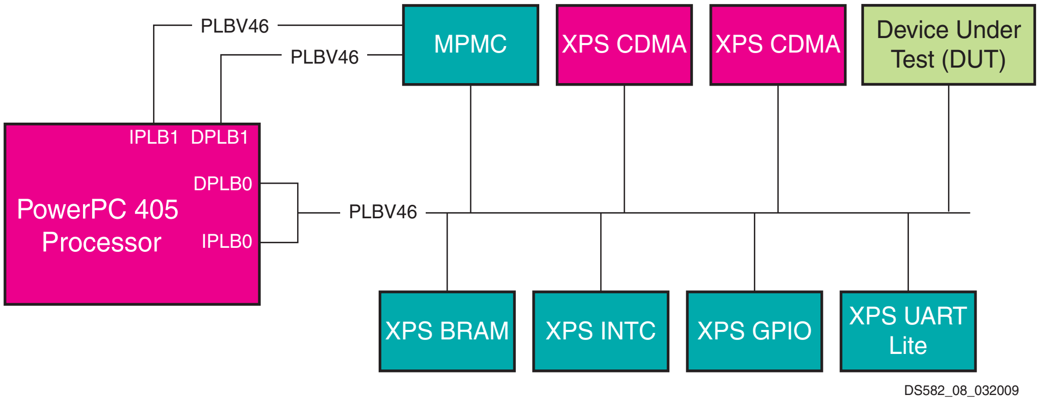

Figure 8: **Virtex-4 FX System**

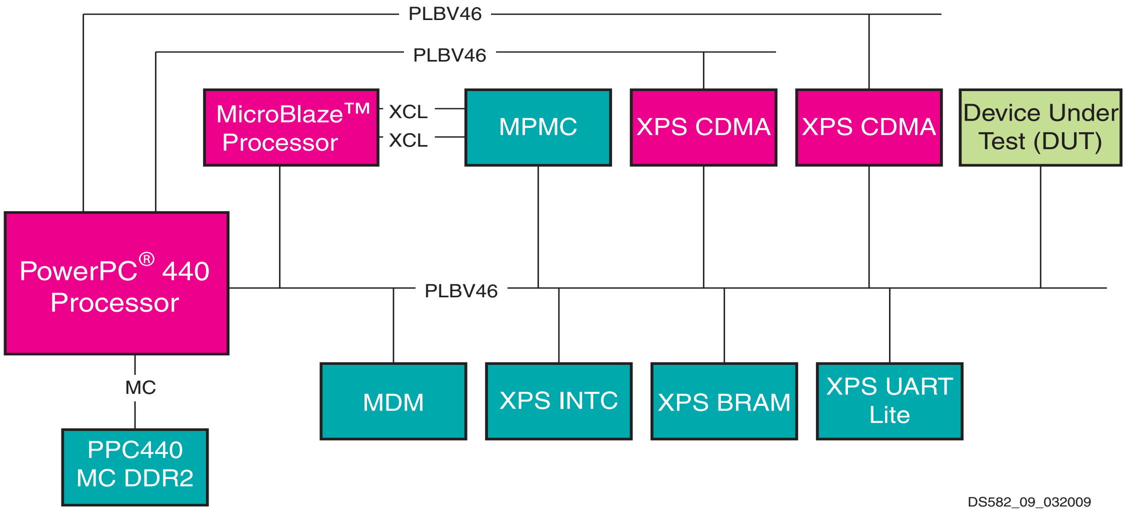

Figure 9: **Virtex-5 FXT System**

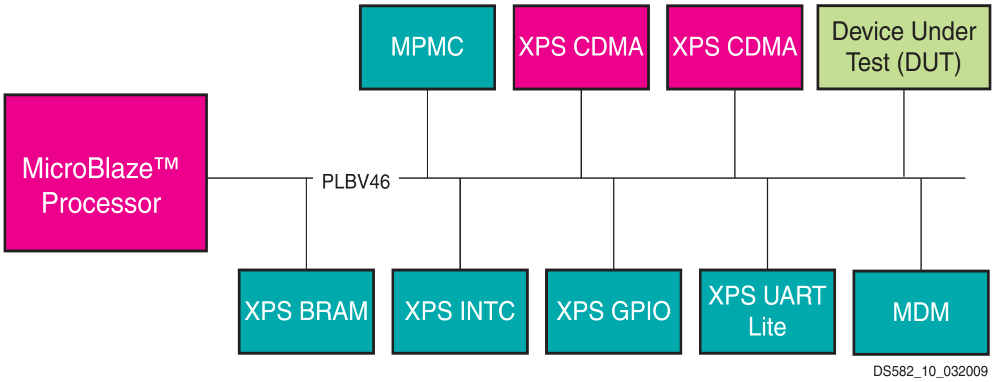

Figure 10: **Spartan-3ADSP System**

The target FPGA was then filled with logic to drive the LUT and BRAM utilization to approximately 70% and the I/O utilization to approximately 80%. Using the default tool options and the slowest speed grade for the target FPGA, the resulting target F_{MAX} numbers are shown in 15.

Table 12: **XPS SYSACE Controller Core System Performance**

Target FPGA	Target F_{MAX} (MHz)
S3D3400 -4	100
V4FX60 -10	125
V5FXT70 -1	150

The target F_{MAX} is influenced by the exact system and is provided for guidance. It is not a guaranteed value across all systems.

Support

Xilinx provides technical support for this LogiCORE product when used as described in the product documentation. Xilinx cannot guarantee timing, functionality, or support of product if implemented in devices that are not defined in the documentation, if customized beyond that allowed in the product documentation, or if changes are made to any section of the design labeled *DO NOT MODIFY*.

Reference Documents

The following documents contain reference information important to understanding the XPS Sysace Controller design:

1. IBM 128-Bit Processor Local Bus, Architecture Specifications, v4.6
2. System Ace:Configuration Solution for Xilinx FPGAs
3. DS080 System ACE Compact Flash Solution

Revision History

Date	Version	Revision
03/08/07	1.0	Initial Xilinx release
10/1/2007	1.2	Added FMax Margin System Performance section; in Table 5, updated Generics G7 and G8 Default Values per CR442353.
11/27/2007	1.3	Added SP-3A DSP support.
1/14/08	1.4	Added Virtex-II Pro support.
4/21/08	1.5	Added Automotive Spartan-3E, Automotive Spartan-3A, and Automotive Spartan-3A DSP support.
7/21/08	1.6	Added QPro Virtex-4 Hi-Rel and QPro Virtex-4 Rad Tolerant support.
10/16/08	1.7	Updated for xps_sysace_v1_01_a version.
4/24/09	1.8	Replaced references to supported device families and tool name(s) with hyperlink to PDF file.
7/20/09	1.9	Added Resource Utilization Tables for S6 / V6 Devices.

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