Utility Differential Signaling Buffer (v1.01a)

Introduction

The Utility Differential Signaling Buffer core generates corresponding buffer to bring off-chip differential signals into internal circuit or out from internal circuits. The core is intended as glue logic between off-chip differential signals and internal circuit.

Features

- Configurable size of the signal width
- Configurable differential signaling buffer type

LogiCORE™ Facts		
Core Specifics		
Supported Device Family	QPro-R Virtex®-II, QPro Virtex-II, Virtex-II, Virtex-II Pro, Virtex-4, QPro Virtex-4QV Hi Rel, QPro Virtex-4 Rad Tolerant, Virtex-5, Spartan®-3	
Version of core	util_ds_buf	v1.01a
Resources Used		
Slices	Min	Max
LUTs	See Table 4.	
FFs		
Block RAMs		
Special Features	None	
Provided with Core		
Documentation	Product Specification	
Design File Formats	VHDL	
Constraints File	UCF	
Verification	VHDL Test bench	
Instantiation Template	VHDL Wrapper	
Reference Designs & application notes	None	
Additional Items	None	
Design Tool Requirements		
Xilinx Implementation Tools	ISE® 9.2i or later	
Verification	N/A	
Simulation	ModelSim SE/EE v6.1e or later	
Synthesis	XST	
Support		
Provided by Xilinx, Inc.		

Functional Description

The Utility Differential Signaling Buffer core generates corresponding buffers to bring off-chip differential signals into or out from internal circuits.

Figure 1 illustrates the Utility Differential Signaling Buffer in a system.

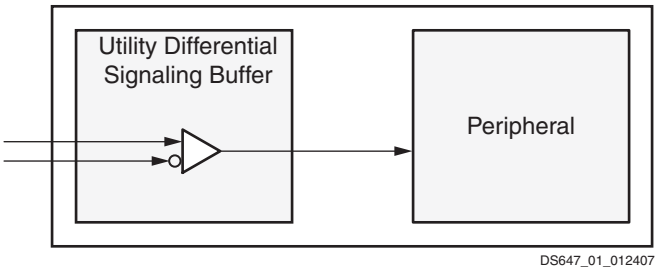

Figure 1: **Utility Differential Signaling Buffer in a System**

I/O Signals

The Utility Differential Signaling Buffer I/O signals are listed and described in Table 1.

Table 1: **Use Initial Caps in Table Title**

Signal	Interface	I/O	Default Value
IBUF_DS_P	None	I	Positive (master) port of the differential input signal: used only for IBUFDS or IBUFGDS.
IBUF_DS_N	None	I	Negative (slave) port of the differential input signal: used only for IBUFDS or IBUFGDS.
IBUF_OUT	None	O	Single ended output signal: used only for IBUFDS or IBUFGDS.
OBUF_IN	None	I	Single ended input signal: used only for OBUFDS.
OBUF_DS_P	None	O	Positive (master) port of the differential output signal, used only for OBUFDS.
OBUF_DS_N	None	O	Negative (slave) port of the differential output signal: used only for OBUFDS.
IOBUF_DS_P	None	IO	Positive (master) port of the differential input signal: used only for IOBUFDS.
IOBUF_DS_N	None	IO	Negative (slave) port of the differential input signal: used only for IOBUFDS.
IOBUF_IO_T	None	I	3-state enable input: used only for IOBUFDS.
IOBUF_IO_I	None	I	3-state buffer input: used only for IOBUFDS.
IOBUF_IO_O	None	O	3-state buffer output: used only for IOBUFDS.

Design Parameters

The Utility Differential Signaling Buffer Parameters are listed and described in Table 2.

Table 2: **Utility Differential Signaling Buffer Parameters**

Parameter	Description	Type
C_SIZE	The vector size of differential signal (valid value is 1 to 128).	integer
C_BUF_TYPE	The differential signaling buffer to be instantiated (valid values are IBUFDS, IBUFGDS, OBUFDS, IOBUFDS, and IBUFDSTXE).	string

Parameter - Port Dependencies

The parameter and port dependencies are listed and described in Table 3.

Table 3: **Utility Differential Signaling Buffer Parameters - Port Dependencies**

Name	Affects	Depends	Relational Description
Design Parameters			
C_SIZE	All signals	0 to C_SIZE-1	Scale width of all port signals
Port Signals			
IBUF_*	All signals	C_BUF_TYPE	Valid for C_BUF_TYPE=IBUFDS or IBUFGDS, not used for other cases
OBUF_*		C_BUF_TYPE	Valid for C_BUF_TYPE=OBUFDS, not used for other cases
IOBUF_*		C_BUF_TYPE	Valid for C_BUF_TYPE=IOBUFDS, not used for other cases

Figure 2 shows three instantiation cases for the core.

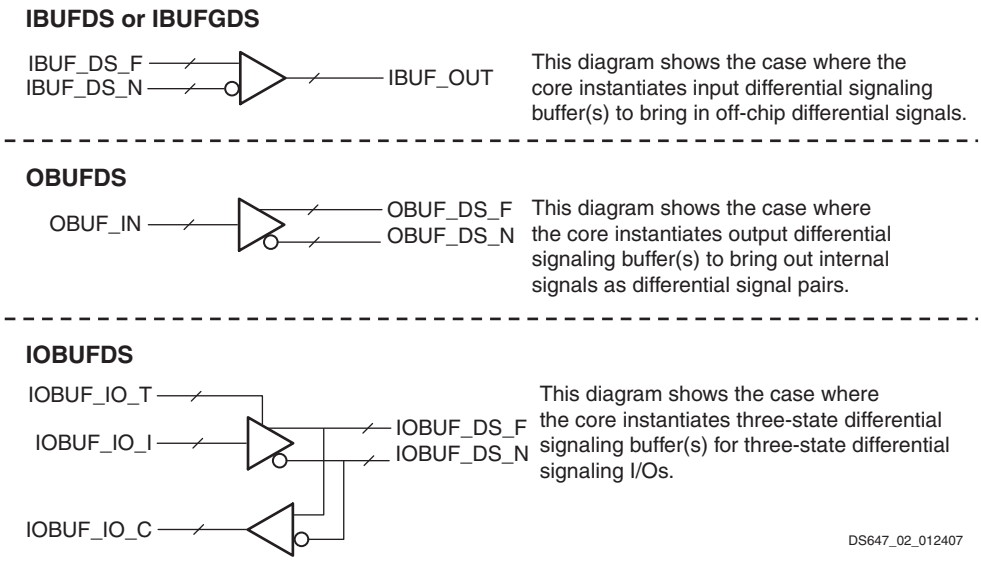

Figure 2: **Utility Vector Logic Block Diagram**

Design Implementation

Design Tools

The Utility Differential Signaling Buffer design is handwritten. Xilinx XST is the synthesis tool used for synthesizing the core.

Target Technology

The target technology is the Virtex and Spartan family FPGAs.

Device Utilization and Performance Benchmarks

Table 4: **Utility Differential Signaling Buffer Resource Utilization**

Parameter		Resources			
		IBUFDS	IBUFGDS	OBUFDS	IOBUFDS
C_SIZE=n	C_BUF_TYPE=IBUFDS	n	0	0	0
	C_BUF_TYPE=IBUFGDS	0	n	0	0
	C_BUF_TYPE=OBUFDS	0	0	n	0
	C_BUF_TYPE=IOBUFDS	0	0	0	n

Reference Documents

None

Revision History

Date	Version	Revision
9/25/07	1.0	Initial Xilinx release.
7/25/08	1.2	Added QPro Virtex-4 Hi-Rel and QPro Virtex-4 Rad Tolerant FPGA support.
9/16/09	1.3	Created v1.01a for EDK_L 11.3 release, incorporated CR530738.

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