MicroBlaze Debug Module (MDM) (v2.00.a)

DS641 July 23, 2010

Product Specification

Introduction

This document provides the design specification for the MicroBlaze™ Debug Module (MDM) which enables JTAG-based debugging of one or more MicroBlaze processors.

Features

- Support for JTAG-based software debug tools
- Support for debugging up to eight MicroBlaze processors (version 7 and higher)
- Support for synchronized control of multiple MicroBlaze processors
- Support for a JTAG-based UART with a configurable AXI4-Lite or PLBv46 interface
- Based on Boundary Scan (BSCAN) logic in Xilinx® FPGAs
- Supports connection to the ChipScope™ Pro ICON core through BSCAN signals

LogiCORE™ IP Facts				
Core Specifics				
Supported Device Family	Spartan®-3, Spartan-3E, Spartan-3A/3A DSP, Automotive Spartan-3/-3A/3A DSP/ 3E, Spartan-6, Virtex®-4, Virtex-4Q, Virtex-4QV, Virtex-5, Virtex-5 FX, Virtex-6, Virtex-6CX[1]			
Resources Used	I/O	LUTs	FFs	Block RAMs
	N/A	4	N/A	N/A
Provided with Core				
Documentation	Product Specification			
Design File Formats	VHDL			
Constraints File	N/A			
Verification	N/A			
Instantiation Template	N/A			
Design Tool Requirements				
Xilinx Implementation Tools	ISE® 12.2 or later			
Verification	N/A			
Simulation	ModelSim PE/SE 6.5c or later			
Synthesis	XST			
Support				
Provided by Xilinx, Inc.				

Notes:

1. S6 and V6 are the only device families that support the AXI4-Lite interface.

Overview

The MicroBlaze Debug Module (MDM):

- Enables JTAG-based debugging of one or more MicroBlaze processors.
- Instantiates one BSCAN primitive. In devices that contain more than one BSCAN primitive, MDM uses the USER2 BSCAN by default.
- Includes a UART with a configurable slave bus interface which can be configured for either an AXI4-Lite interconnect or a PLBv46 bus.

The UART TX and RX signals are transmitted over the FPGA JTAG port to and from the Xilinx Microprocessor Debug (XMD) tool. The UART behaves in a manner similar to the LogiCORE IP AXI (UART) Lite core.

The block diagram of the module is shown in Figure 1:

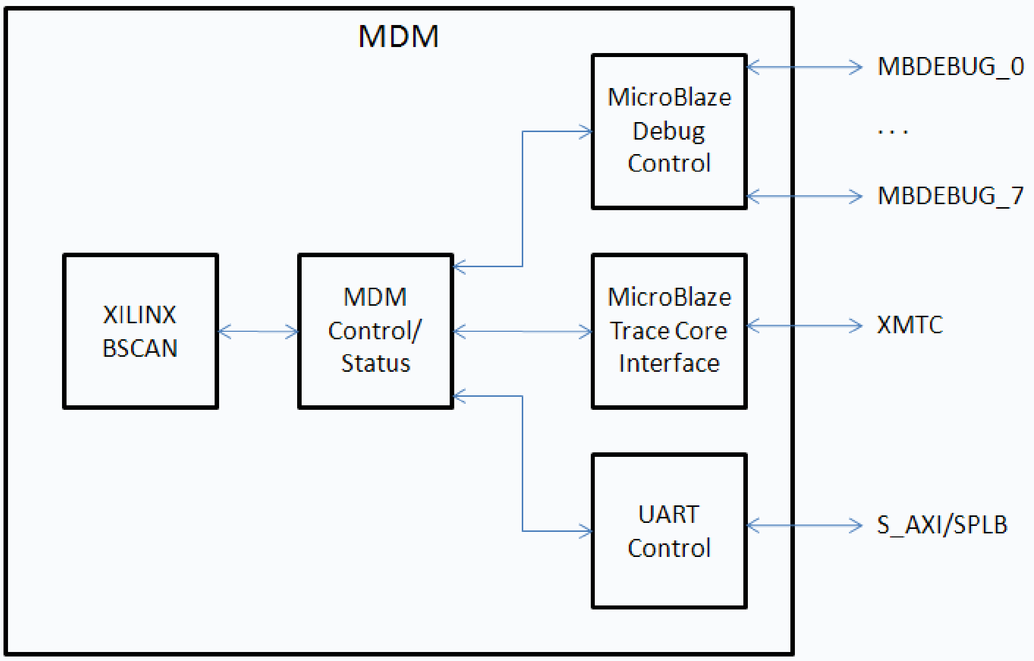

Figure 1: **Microblaze Debug Module (MDM) Block Diagram**

MDM I/O Signals

The I/O signals for the MicroBlaze Debug Module (MDM) are listed and described in Table 1.

Table 1: **MDM I/O Signals**

Signal Name	Interface	I/O	Initial State	Description
System Signals				
Interrupt		O	0	Interrupt from UART
Debug_SYS_Rst		O	0	Debug system reset
Ext_BRK		O	0	External break
Ext_NM_BRK		O	0	External non-maskable break
PLB Interface Signals				
SPLB_Clk	SPLB	I	-	PLB clock
SPLB_Rst	SPLB	I	-	PLB reset
PLB_ABus[0:31]	SPLB	I	-	PLB address bus
PLB_UABus[0:31]	SPLB	I	-	PLB upper address bus
PLB_PAValid	SPLB	I	-	PLB primary address valid
PLB_SAValid	SPLB	I	-	PLB secondary address valid
PLB_rdPrim	SPLB	I	-	PLB secondary to primary read request indicator
PLB_wrPrim	SPLB	I	-	PLB secondary to primary write request indicator
PLB_MasterID[0:C_SPLB_MID_WIDTH-1]	SPLB	I	-	PLB current master identifier
PLB_busLock	SPLB	I	-	PLB bus lock
PLB_abort	SPLB	I	-	PLB abort
PLB_RNW	SPLB	I	-	PLB read not write
PLB_BE[0:C_SPLB_DWIDTH/8 - 1]	SPLB	I	-	PLB byte enables
PLB_MSize[0:1]	SPLB	I	-	PLB data bus width indicator
PLB_size[0:3]	SPLB	I	-	PLB size of requested transfer
PLB_type[0"2]	SPLB	I	-	PLB transfer type
PLB_lockErr	SPLB	I	-	PLB lock error
PLB_wrDBus[0:C_SPLB_DWIDTH-1]	SPLB	I	-	PLB write data bus
PLB_wrBurst	SPLB	I	-	PLB burst write transfer
PLB_rdBurst	SPLB	I	-	PLB burst read transfer
PLB_wrPendReq	SPLB	I	-	PLB pending bus write request
PLB_rdPendReq	SPLB	I	-	PLB pending bus read request
PLB_wrPendPri[0:1]	SPLB	I	-	PLB pending write request priority
PLB_rdPendPri[0:1]	SPLB	I	-	PLB pending read request priority
PLB_reqPri[0:1]	SPLB	I	-	PLB current request priority
PLB_TAttribute[0:15]	SPLB	I	-	PLB transfer attribute
Sl_addrAck	SPLB	O	-	Slave address acknowledge
Sl_SSize[0:1]	SPLB	O	-	Slave data bus size

Table 1: **MDM I/O Signals** ***(Cont'd)***

Signal Name	Interface	I/O	Initial State	Description
Sl_wait	SPLB	O	-	Slave wait
Sl_rearbitrate	SPLB	O	-	Slave bus re-arbitrate
Sl_wrDAck	SPLB	O	-	Slave write data acknowledge
Sl_wrComp	SPLB	O	-	Slave write transfer complete
Sl_wrBTerm	SPLB	O	-	Slave terminate write burst transfer
Sl_rdDBus[0:C_SPLB_DWIDTH -1]	SPLB	O	-	Slave read data bus
Sl_rdWdAddr[0:3]	SPLB	O	-	Slave read word address
Sl_rdAck	SPLB	O	-	Slave read data acknowledge
Sl_rdComp	SPLB	O	-	Slave read transfer complete
Sl_rdBTerm	SPLB	O	-	Slave terminate read burst transfer
Sl_MBusy [0:C_SPLB_NUM_MASTERS-1]	SPLB	O	-	Slave busy
Sl_MWrErr [0:C_SPLB_NUM_MASTERS-1]	SPLB	O	-	Slave write error
Sl_MrdErr [0:C_SPLB_NUM_MASTERS-1]	SPLB	O	-	Slave read error
Sl_MIRQ [0:C_SPLB_NUM_MASTERS-1]	SPLB	O	-	Master interrupt request
AXI4-Lite Interface Signals				
S_AXI_ACLK	S_AXI	I	-	AXI Clock
S_AXI_ARESETN	S_AXI	I	-	AXI Reset, active low
S_AXI_AWADDR[C_S_AXI_ADDR_WIDTH-1:0]	S_AXI	I	-	Write Address
S_AXI_AWVALID	S_AXI	I	-	Write Address Valid
S_AXI_AWREADY	S_AXI	O	0	Write Address Ready
S_AXI_AWDATA[C_S_AXI_DATA_WIDTH-1:0]	S_AXI	I	-	Write Data
S_AXI_AWSTB[C_S_AXI_DATA_WIDTH/8-1:0]	S_AXI	I	-	Write Strobes
S_AXI_WVALID	S_AXI	I	-	Write Valid
S_AXI_WREADY	S_AXI	O	0	Write Ready
S_AXI_BRESP[1:0]	S_AXI	O	0	Write Response
S_AXI_BVALID	S_AXI	O	0	Write Response Valid
S_AXI_BREADY	S_AXI	I	-	Write Response Ready
S_AXI_ARADDR[C_S_AXI_ADDR_WIDTH-1:0]	S_AXI	I	-	Read Address
S_AXI_ARVALID	S_AXI	I	-	Read Address Valid
S_AXI_ARREADY	S_AXI	O	0	Read Address Ready
S_AXI_RRESP[1:0]	S_AXI	O	0	Read Response
S_AXI_RVALID	S_AXI	O	0	Read Valid
S_AXI_RREADY	S_AXI	I	-	Read Ready
MicroBlaze Debug Interface Signals				
Dbg_Clk_n	MBDEBUG_n	O	0	MicroBlaze Debug Clock

Table 1: **MDM I/O Signals** ***(Cont'd)***

Signal Name	Interface	I/O	Initial State	Description
Dbg_TDI_n	MBDEBUG_n	O	0	MicroBlaze Debug TDI
Dbg_TDO_n	MBDEBUG_n	I	-	MicroBlaze Debug TDO
Dbg_Reg_En_n	MBDEBUG_n	O	0	MicroBlaze Debug Register Enable
Dbg_Capture_n	MBDEBUG_n	O	0	MicroBlaze Debug Capture
Dbg_Shift_n	MBDEBUG_n	O	0	MicroBlaze Debug Shift
Dbg_Update_n	MBDEBUG_n	O	0	MicroBlaze Debug Update
Dbg_Rst_n	MBDEBUG_n	O	0	MicroBlaze Debug Reset
MicroBlaze Trace Core Interface Signals				
Ext_JTAG_DRCK	XMTC	O	0	Connection to MicroBlaze Trace Core
Ext_JTAG_RESET	XMTC	O	0	Connection to MicroBlaze Trace Core
Ext_JTAG_SEL	XMTC	O	0	Connection to MicroBlaze Trace Core
Ext_JTAG_CAPTURE	XMTC	O	0	Connection to MicroBlaze Trace Core
Ext_JTAG_SHIFT	XMTC	O	0	Connection to MicroBlaze Trace Core
Ext_JTAG_UPDATE	XMTC	O	0	Connection to MicroBlaze Trace Core
Ext_JTAG_TDI	XMTC	O	0	Connection to MicroBlaze Trace Core
Ext_JTAG_TDO	XMTC	I	-	Connection to MicroBlaze Trace Core
Chipscope ICON Interface Signals				
bscan_tdi	ICON	O	0	Connection to Chipscope ICON core
bscan_reset	ICON	O	0	Connection to Chipscope ICON core
bscan_shift	ICON	O	0	Connection to Chipscope ICON core
bscan_update	ICON	O	0	Connection to Chipscope ICON core
bscan_capture	ICON	O	0	Connection to Chipscope ICON core
bscan_sel1	ICON	O	0	Connection to Chipscope ICON core
bscan_drck1	ICON	O	0	Connection to Chipscope ICON core
bscan_tdo1	ICON	I	-	Connection to Chipscope ICON core

MDM Design Parameters

Table 2 lists and describes the features that can be parameterized in MDM.

Table 2: **MDM Design Parameters**

Feature / Description	Parameter Name	Allowable Values	Default Value	VHDL Type
System Parameters				
Target FPGA family	C_FAMILY	spartan3, aspartan3, spartan3e, aspartan3e, spartan3a, aspartan3a, spartan3adsp, aspartan3adsp, spartan6, virtex4, qrvirtex4, qvirtex4, virtex5, virtex5fx, virtex6, virtex6cx	virtex5	string
Debug Parameters				
Number of MicroBlaze debug ports	C_MB_DBG_PORTS	0-8	1	integer
Position in the FPGA JTAG chain	C_JTAG_CHAIN	1 = USER1 2 = USER2 3 = USER3 4 = USER4	2	integer
UART Parameters				
Enables the UART interface	C_USE_UART	0,1	1	integer
Selects the bus interface for the UART	C_INTERCONNECT	1 = PLBv46, 2 = AXI	1	integer
UART Base Address	C_BASEADDR	Valid Address(1)	None (1)	std_logic_vector
UART High Address	C_HIGHADDR	Valid Address (1)	None (1)	std_logic_vector
PLB Parameters				
PLB address width	C_SPLB_AWIDTH	32	32	integer
PLB data width	C_SPLB_DWIDTH	32	32	integer
Selects point-to-point or shared PLB topology	C_SPLB_P2P	0 = Shared Bus Topology 1 = Point-to-Point Bus Topology	0	integer
PLB MAster ID Bus Width	C_SPLB_MID_WIDTH	log$_2$ (C_SPLB _NUM_MASTERS) with a minimum value of 1	1	integer
Number of PLB Masters	C_SPLB_NUM_ MASTERS	1-16	1	integer
Width of the Slave Data Bus	C_SPLB_NATIVE_WIDTH	32	32	integer
Selects the transactions as being single beat or burst	C_SPLB_SUPPORT_ BURSTS	0 = Supports only single beat transactions	0	integer
AXI4-Lite Parameters				
AXI Address Bus Width	C_S_AXI_ADDR_WIDTH	32	32	integer
AXI Data Bus Width	C_S_AXI_DATA_WIDTH	32	32	integer

1. The range specified by C_BASESADDR and C_HIGHADDR must be sized and aligned to some power of 2, 2n. Then, the least n significant bits of C_BASEADDR are zero. This range needs to encompass the addresses needed by the MDM UART registers.

Allowable Parameter Combinations

There are no restrictions on parameter combinations for this core.

Parameter-Port Dependencies

The core has no parameter-port dependencies.

MDM Registers

The MDM registers are listed and described in Table 3.

Table 3: **MDM Registers**

Register Name	Size (bits)	Address Offset	Initial State	Description
Rx_FIFO	C_UART_WIDTH	0	0	JTAG UART receive data
Tx_FIFO	C_UART_WIDTH	4	0	JTAG UART transmit data
Status_reg	8	8	0x04	Read only bit 7 rx_Data_Present bit 6 rx_Buffer_Full bit 5 tx_Buffer_Empty bit 4 tx_Buffer_Full bit 3 enable_interrupts
Ctrl_reg	8	C	0x03	Write only bit 3 enable_interrupts bit 5 Clear Ext BRK signal bit 6 Reset_RX_FIFO bit 7 Reset_TX_FIFO

MDM Interrupts

If the interrupt enable register bit in the control register is set, the UART raises the interrupt signal in the cycle when the TX FIFO goes empty, or in every cycle where the RX FIFO has data available.

Design Implementation

Target Technology

The target technology is an FPGA listed in the Supported Device Family field of the LogiCORE IP Facts Table.

Device Utilization and Performance Benchmarks

Not available.

Specification Exceptions

When programming a System Ace device, the MDM clock must be at least twice as fast as the System Ace™ tool controller clock for the ELF file to load correctly.

Reference Documents

The MDM core is intended to be used with the EDK XMD tool. For more information on how to debug using MDM and XMD, see the *Embedded System Tools Reference Manual*.

Revision History

The following table shows the revision history for this document:

Date	Version	Revision
06/18/07	1.0	Initial Xilinx release.
11/21/07	1.1	Updated table titles.
04/28/08	1.2	Added Automotive Spartan®-3E, Automotive Spartan-3A, Automotive Spartan-3 and Automotive Spartan-3A DSP; added Spartan-3A DSP.
06/25/08	1.3	Added QPro Virtex4 Hi-Rel and QPro Virtex4 Rad Tolerant.
08/27/08	1.4	Remove Virtex-II Pro.
12/15/08	1.5	In LogiCORE IP Facts Table, replaced device family listing and tool name(s) with link to PDF file; added link to special disclaimer on first page.
04/24/09	1.6	Replaced references to supported device families and tool name(s) with hyperlink to PDF file. Removed references to fast download.
6/24/09	1.7	Updated for EDK_L 11.2; created version 1.00f.
12/02/09	1.8	Created version 1.00g for the 11.4 build.
12/15//09	1.9	Incorporated CR540684 to correct link to Embedded System Tools Reference Manual on page 8.
07/23/10	2.0	Xilinx 12.2 release.

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